Digital Logic Design Laboratory

Lab 6

Flip Flops and Counters

Full name: Phan Tiến Đạt

Student number: EEACIU22170

Class: ……………………………………………….......

Date: …………………………………………………....

# I. Objectives

In this laboratory, students will study:

- Understand the operation of Flip Flops.

- Use a Flip Flops and design/implement a circuit based on a function definition.

- Design a counter based on Flip Flops

# II. Procedure

1. Investigate Flip Flops (FF)

Flip flops are one of the most fundamental electronic components. These are used as one-bit storage elements, clock dividers and it can make counters, shift registers and storing registers by connecting the flip flops in particular sequences.

a. JK- Flip Flops

Given the JK Flip Flop as shown in Figure 1. The J-K flip-flop is the most versatile of the basic flip-flops. It has two inputs, traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge.

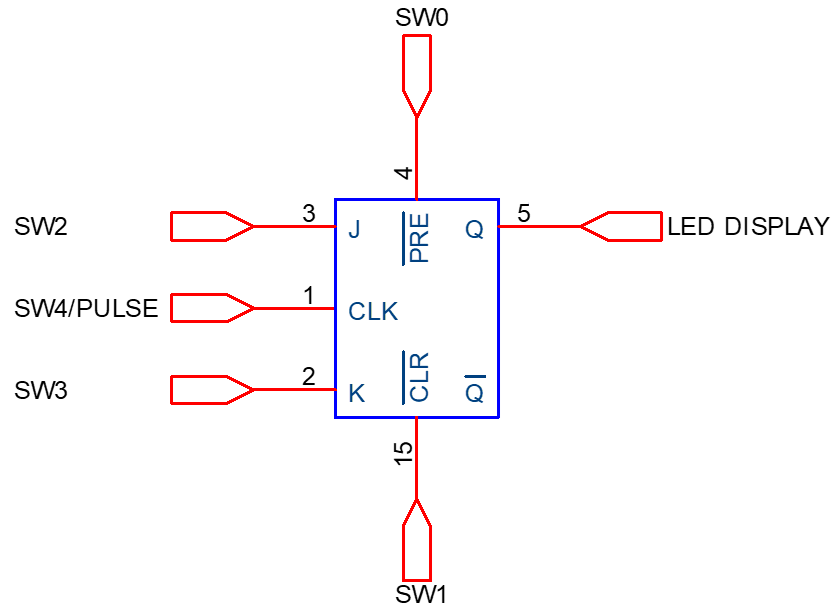


Figure 1. JK Flip Flop

Built the truth table:

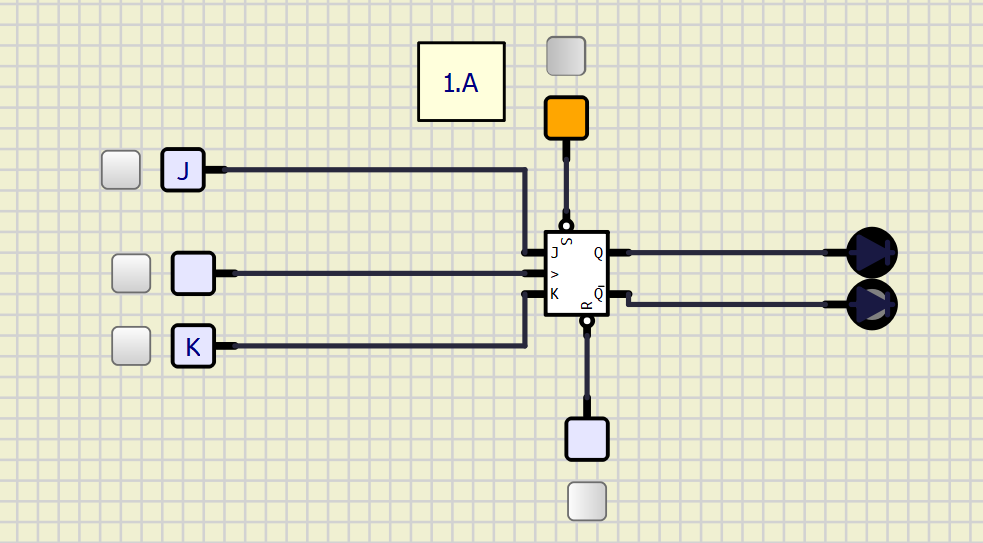
|  |  |  |  |
| --- | --- | --- | --- |
| J | K | CLK | Q+ |
| 0 | 0 | ↑ | No change |
| 0 | 1 | ↑ | 0 |
| 1 | 0 | ↑ | 1 |
| 1 | 1 | ↑ | No change |

What is the usage of  and ?

: when is active Q is immediately set to 1

:when is active Q is reset to 0.

Implement the circuit (Figure 1) via simulation software and paste the result in here



b. D- Flip Flops

The D flip-flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell.

Figure 2. D Flip FDiagram, schematic

Description automatically generatedlop

Built the truth table:

|  |  |  |
| --- | --- | --- |
| D | CLK | Q+ |
| 0 | ↑ | 0 |
| 1 | ↑ | 1 |

What is the usage of  and ?





Implement the circuit (Figure 2) via simulation software and paste the result in here

A computer screen shot of a diagram

Description automatically generated

c. Convert JK-FF into D-FF

From the block diagram shown in figure 3, design the circuit to convert J K-FF to D-FF:

Diagram

Description automatically generated

Figure 3. Convert JK-FF into D-FF

Implement the circuit via simulation software and paste the result in here

A diagram of a computer

Description automatically generated

Make comment on the results

2. Analyze and design asynchronous counters

a. Implement an asynchronous up counter having M = 8 using J-K Flip Flop

Implement the below circuit in Figure 4. Control  (SW1) and (SW2) to make the circuit operate.

Diagram, schematic

Description automatically generated

Figure 4. Logic diagram

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a computer diagram

Description automatically generated

Make comment on the results

Implement the circuit via simulation software and paste the result in here

c. Implement an asynchronous 3-bit down counter having M = 8 by using J-K Flip Flop

Implement the below circuit shown in Figure 5. The  (SW1) and (SW2) inputs are in the appropriate states to make the circuit operate:

Diagram, schematic

Description automatically generated

Figure 5. Logic diagram

Implement the circuit via simulation software and paste the result in here

Make comment on the results

d. Implement an asynchronous 3-bit counter having M = 8, with a control for up/down counting.

Implement the below circuit shown in Figure 6. The  (SW1) and (SW2) inputs are in the appropriate states to make the circuit operate:

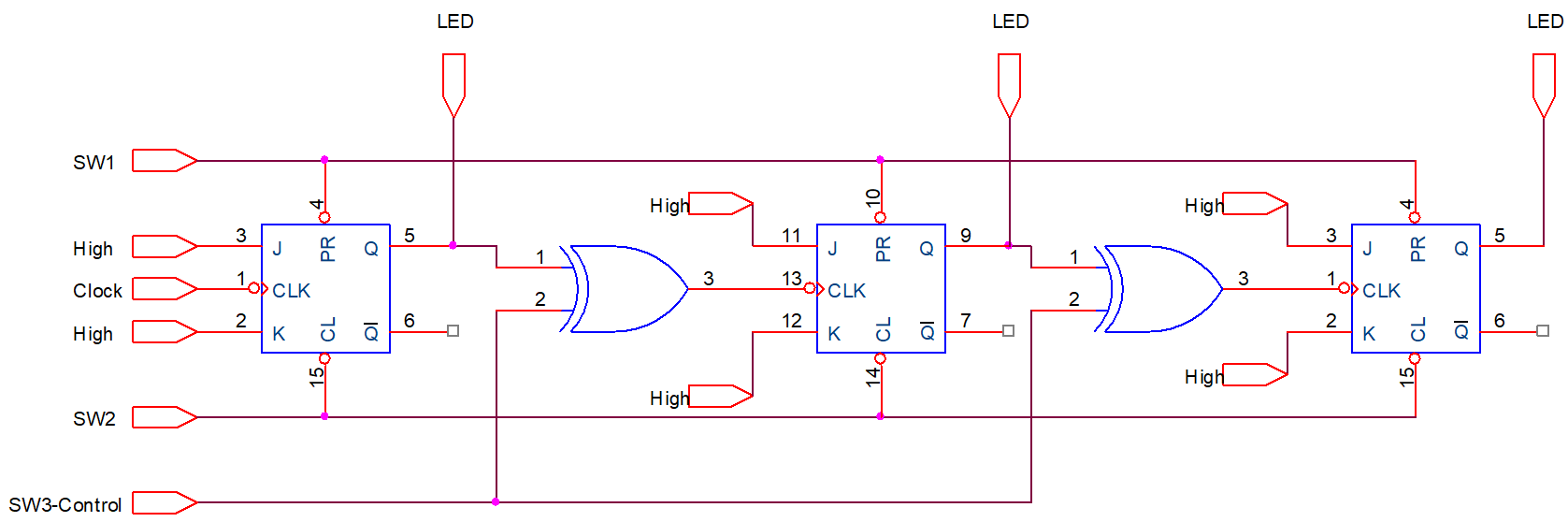


Figure 6. Logic diagram

Implement the circuit via simulation software and paste the result in here

Make comment on the results

3. Analyze and design synchronous counters

a. Analyze the counter given schematic circuit

Implement the below circuit in Figure 7. Control  (SW1) and (SW2) to make the circuit operate.

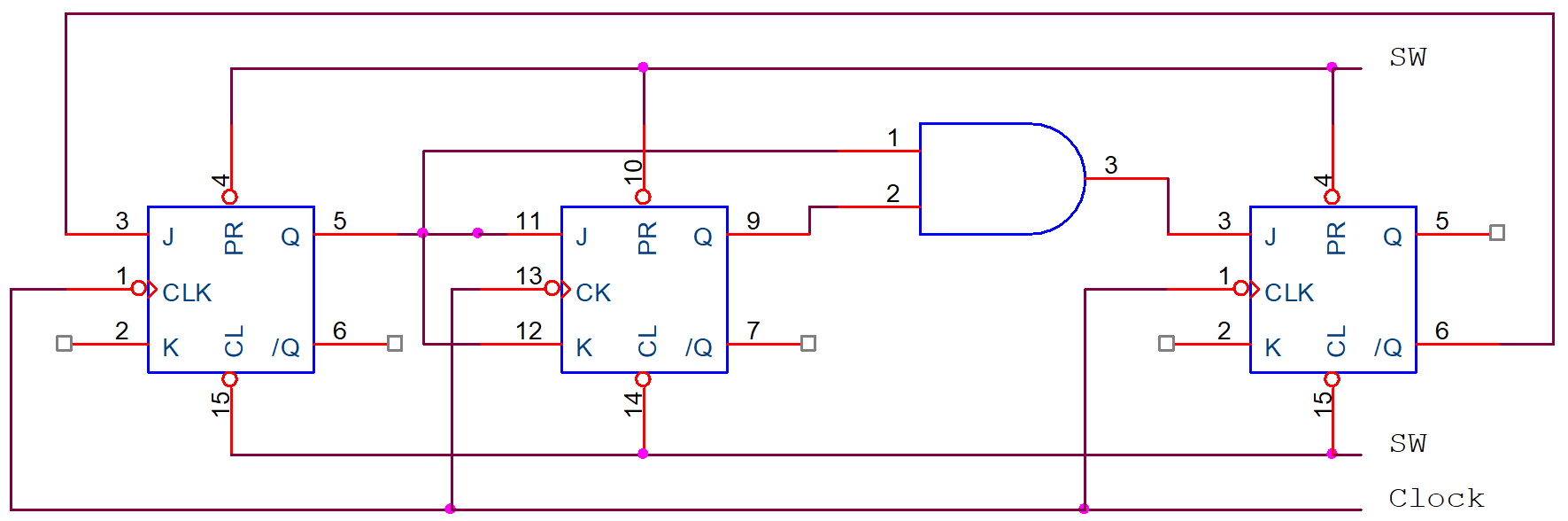


Figure 7. Logic diagram

When the clock is active:

…………………………………………………………………………………………………………………………………………………………………………………….

Write the excitation (trigger) input equations of all flip-flops:

J0 = …………………...............; K0 = ….……………...............

J1 = …………………...............; K1 = ….……………...............

J2 = …………………...............; K2 = ….……………...............

Transition Table

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | | |  | | | | | | Next State | | |
| Q2 | Q1 | Q0 | J2 | K2 | J1 | K1 | J0 | K0 | Q2 | Q1 | Q0 |
| 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |
| 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |

Implement the circuit via simulation software and paste the result in here

Draw the state diagram of the counter

Make comment on the results

b. Design and implement a synchronous counter by the given state diagram

Design and implement a synchronous 2-bit counter shown in the given diagram as shown in Figure 8 using J-K Flip Flops

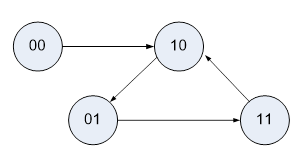


Figure 8. State diagram

Transition Table

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | |  | | | | Next State | |
| Q1 | Q0 | J1 | K1 | J0 | K0 | Q1 | Q0 |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

Write the excitation (trigger) input equations of all flip-flops:

J0 = …………………...............; K0 = ….……………...............

J1 = …………………...............; K1 = ….……………...............

Implement the circuit via simulation software and paste the result in here

Make comment on the results